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What is claimed is:

1. A DC canceler circuit comprising:
 - a. a canceler input terminal adapted to receive a series of data input samples $x(n)$;
 - b. a canceler output terminal adapted to provide a series of data output samples $y(n)$;
 - c. a feedback path having:
 - i. a feedback-path input terminal connected to the canceler output terminal;
 - ii. a feedback-path output terminal connected to the canceler input terminal; and
 - iii. a sigma-delta modulator having a sigma-delta input terminal connected to the feedback-path input terminal and a sigma-delta output terminal connected to the feedback-path output terminal.
2. The canceler circuit of claim 1, further comprising a subtractor having a first subtractor input node connected to the canceler input terminal and a second subtractor input node connected to the sigma-delta output terminal.
3. The canceler circuit of claim 1, further comprising a unit delay element having a delay-element input terminal connected to the feedback path input terminal and a delay-element output terminal connected to the sigma-delta input terminal.

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1 4. The canceler circuit of claim 3, further comprising an
2 adder having a first adder input terminal connected to
3 the delay-element output terminal, a second adder input
4 terminal connected to the feedback path input terminal,
5 and an adder output terminal connected to the delay-
6 element input terminal.

7
8 5. The canceler circuit of claim 4, wherein the adder
9 connects to the feedback path input terminal via a
10 multiplier.

11
12 6. A receiver comprising:
13 a. a processing chip configured to include;
14 i. a data input port;
15 ii. a data output port;
16 iii. sigma-delta modulator connected to the data
17 input port and having a control-signal output
18 port; and
19 b. a feedback path connected between the control-
20 signal output port and the data input port.

21
22 7. The receiver of claim 6, wherein the feedback path
23 includes:
24 a. an analog component having a filter input
25 terminal; and
26 b. an analog filter connected between the control-
27 signal output port and the filter input terminal.

28
29 8. The receiver of claim 7, wherein the analog component
30 includes an automatic gain control circuit.

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- 1 9. The receiver of claim 7, wherein the analog component
2 includes a voltage-controlled oscillator.
3
- 4 10. The receiver of claim 6, wherein the processing chip is
5 programmable logic device.
6
- 7 11. The receiver of claim 10, wherein the programmable
8 logic device is a field programmable gate array.
9
- 10 12. A sigma-delta loop having a tunable center frequency,
11 the loop comprising:
12 a. a data input terminal adapted to receive data
13 $x(n)$;
14 b. a tunable all-pass network having an all-pass
15 network input terminal connected to the data input
16 terminal and an all-pass network output terminal;
17 c. a global feedback network connected between the
18 all-pass network output terminal and the all-pass
19 network input terminal; and
20 d. a local feedback network connected between the
21 all-pass network output terminal and the all-pass
22 network input terminal.
23
- 24 13. The sigma-delta loop of claim 12, further comprising a
25 second tunable all-pass network having a second all-
26 pass network input terminal, connected to the first-
27 mentioned all-pass network output terminal, and a
28 second all-pass network output terminal.
29
- 30 14. The sigma-delta loop of claim 12, wherein the global
31 feedback network comprises:
32 a. a first co-efficient multiplier connected between

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1 the first-mentioned all-pass network output
2 terminal and the first-mentioned all-pass network
3 input terminal; and
4 b. a second co-efficient multiplier connected between
5 the second all-pass network output terminal and
6 the first-mentioned all-pass network input
7 terminal.

8
9 15. The sigma-delta loop of claim 14, further comprising a
10 quantizer having a quantizer input terminal connected
11 to the global feedback network and a quantizer output
12 terminal connected to the first-mentioned all-pass
13 network input terminal.

14
15 16. A tunable sigma-delta loop comprising:
16 a. a data input terminal adapted to receive data
17 $x(n)$;
18 b. a first subtractor having a first input terminal,
19 a second input terminal, and an output terminal;
20 c. a second subtractor having a first input terminal
21 connected to the output terminal of the first
22 subtractor, a second input terminal, and an output
23 terminal;
24 d. a first adder having a first input terminal
25 connected to the output terminal of the second
26 adder, a second input terminal, and an output
27 terminal;
28 e. a tunable all-pass network having an all-pass
29 network input terminal connected to the output
30 terminal of the first adder and an all-pass
31 network output terminal connected to the second
32 input terminal of the first adder;

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- 1 f. a local feedback network having a local-feedback
2 input terminal connected to the all-pass network
3 output terminal and a local-feedback output
4 terminal connected to the second input terminal of
5 the of the second subtractor;
- 6 g. a global feedback network having a global-feedback
7 input terminal connected to the all-pass network
8 output terminal and a global-feedback output
9 terminal; and
- 10 h. a quantizer having a quantizer input terminal
11 connected to the global-feedback output terminal
12 and a quantizer output terminal connected to the
13 second input terminal of the first subtractor.
14
- 15 17. The loop of claim 16, further comprising:
- 16 a. a second adder having a first adder input terminal
17 connected to the first-mentioned all-pass network
18 output terminal, a second adder input terminal,
19 and an adder output terminal connected to the
20 local-feedback input terminal;
- 21 b. a second tunable all-pass network having an all-
22 pass network input terminal connected to the
23 output terminal of the second adder and a all-pass
24 network output terminal connected to the second
25 input terminal of the second adder;
- 26 c. a second global feedback network having a global-
27 feedback input terminal connected to the all-pass
28 network output terminal of the second all-bass
29 network and a global-feedback output terminal;
- 30 d. a third adder having a first input terminal
31 connected to the global-feedback output terminal
32 of the first-mentioned global feedback network, a

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1 second input terminal connected to the global-
2 feedback output terminal of the second global
3 feedback network, and an output terminal connected
4 to the quantizer input terminal.
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